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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DUDEK, JAMES A	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,749	HONG ET AL.	
	Examiner	Art Unit	
	James A. Dudek	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2 and 7-10 is/are rejected.

7)☒ Claim(s) 3-6 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/676,813.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,299,041 (041) in view of US 20010035919 A1, US 6532050 B1, US 5995174 A, US 5986725 A, US 5978058 A, US 5977563 A, US 5926242 A, US 5926235 A, US 5923390 A, US 5883682 A, US 5852488 A, US 5847781 A and US 5818550 A.

041 teaches a thin film transistor array panel for a liquid crystal display, comprising: an insulating substrate including a display area [area up to the pixels electrodes at the edges of the matrix], a peripheral area around a circumference of the display area [the area corresponding to the black matrix surrounding the display area, see figure 3], and an outer area comprising other than the display area and the peripheral area [the area corresponding to the seal]; a black matrix formed on the display area of the insulating substrate and having an opening of a matrix array corresponding to pixels [126]; red, blue and green color filters formed at the pixels on the insulating substrate [124]; an insulating layer covering the black matrix and the color filters [128]; and a pixel wire including a pixel electrode [10].

041 lacks a gate wire including a gate line and a gate electrode connected to the gate line, and formed on the insulating layer; a gate insulating layer covering the gate wire on the insulating layer; a semiconductor pattern formed on the gate insulating layer; a data wire including a source electrode and a drain electrode that are made of a same layer on the semiconductor pattern and separated from each other, and a data line connected to the source electrode and defining a pixel in a matrix array by crossing the gate line; a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; the pixel electrode connected to the drain electrode through the first contact hole. However, it was well known to use TFTs having a gate line and a gate electrode connected to the gate line, and formed on the insulating layer; a gate insulating layer covering the gate wire on the insulating layer; a semiconductor pattern formed on the gate insulating layer; a data wire including a source electrode and a drain electrode that are made of a same layer on the semiconductor pattern and separated from each other, and a data line connected to the source electrode and defining a pixel in a matrix array by crossing the gate line; a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; the pixel electrode connected to the drain electrode through the first contact hole for several reasons including improved resolution. Furthermore, US 20010035919 A1, US 6532050 B1, US 5995174 A, US 5986725 A, US 5978058 A, US 5977563 A, US 5926242 A, US 5926235 A, US 5923390 A, US 5883682 A, US 5852488 A, US 5847781 A and US 5818550 A evidence it was well known. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the well known TFT with 041.

041 teaches the thin film transistor array panel of claim 1, but lacks the edges of the red, green and blue color filters overlap the black matrix. However, this was well known for improving contrast. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention.

041 teaches the thin film transistor array panel of claim 1, but lacks the insulating layer is planar and is made of organic insulating material. However, it was well known to use organic materials to simplify manufacturing of forming a planar layer and it was well known to flatten the passivation layer to decrease the noise of the cell. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention.

041 teaches the thin film transistor array panel of claim 1, but lack the black matrix, the gate wire, or the data wire have a single-layered structure made of aluminum, aluminum alloy, copper or copper alloy, or multi-layered structure including a conductive material of chromium, molybdenum, molybdenum alloy, chromium nitride or molybdenum nitride. However, it was well known to from any of the black matrix, gate or source from aluminum or aluminum alloy or copper etc. in order to improve conductivity and light blocking capabilities. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention.

Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,299,041 (041) in view of US 20010035919 A1, US 6532050 B1, US 5995174 A, US 5986725 A, US 5978058 A, US 5977563 A, US 5926242 A, US 5926235 A, US 5923390 A, US 5883682 A, US 5852488 A, US 5847781 A and US 5818550 A, as applied to claim 1 above and further in view of US006400440B1 (440).

041 teaches the thin film transistor array panel of claim 2, but lacks an alignment key formed of a same layer as the black matrix or the color filters of the outer area. However, 440 teaches alignment marks formed from the black matrix to align the TFT plate 15 with an accuracy of better than 3 microns (usually within 1 micron). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention.

Claims 2 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US006532050B1 (050) in view of 440.

050 teaches the thin film transistor array panel of claim 2, but lacks an alignment key formed of a same layer as the black matrix or the color filters of the outer area. However, 440 teaches alignment marks formed from the black matrix to align the TFT plate 15 with an accuracy of better than 3 microns (usually within 1 micron). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention.

050 teaches the thin film transistor array panel of claim 1, but lack the black matrix, the gate wire, or the data wire have a single-layered structure made of aluminum, aluminum alloy, copper or copper alloy, or multi-layered structure including a conductive material of chromium, molybdenum, molybdenum alloy, chromium nitride or molybdenum nitride. However, it was

well known to from any of the black matrix, gate or source from aluminum or aluminum alloy or copper etc. in order to improve conductivity and light blocking capabilities. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 7-8... are rejected under 35 U.S.C. 102(e) as being clearly anticipated by US006532050B1.

Allowable Subject Matter

Claims 3-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A. Dudek whose telephone number is 571-272-2290. The examiner can normally be reached on 9:00-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James A. Dudek
Primary Examiner
Art Unit 2871